

**REMARKS**

Claims 1-12, 14, 16, 18 and 19 are pending in this application, all of which stand rejected.

**Claims 1, 5, 12, 16, 18 and 19 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hammond et al. in view of IBM Technical Disclosure Bulletin, *Instruction Cache Bypass During Cache Reload* (“IBM”).**

With respect to **independent claims 1 and 12**, the Examiner admitted that Hammond et al. does not explicitly teach the claimed selector. However, the Examiner applied IBM, and asserted that the reference teaches the missing feature. In more detail, the Examiner asserted that IBM teaches selecting either an instruction stored in an instruction cache or an instruction from a main memory based on if there is a cache miss so as to reduce the delay associated with waiting for an instruction while a cache line is being retrieved on a cache miss. The Examiner concluded that it would have been obvious to modify Hammond’s processor based on the teaching of IBM to arrive at the claimed invention. The Examiner’s asserted motivation to modify Hammond’s processor is that instructions can be selected from either the output of the translator or the instruction cache based on a cache hit/miss in order to reduce the delay associated with a cache miss. See paragraphs 5, 6, 9 and 10 of the Office Action. This rejection is respectfully traversed.

In imposing a rejection under 35 U.S.C. §103, the Examiner is required to make a “thorough and searching” factual inquiry and, based upon such a factual inquiry, explain why one having ordinary skill in the art would have been realistically impelled to modify particular prior art, in this case Hayashi’s particular semiconductor device, to arrive at the claimed invention. *In re Lee*, 277 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). Merely

identifying features of a claimed invention in disparate prior art references does not, automatically, establish the requisite motivation for combining references in any particular manner. *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999); *Grain Processing Corp. v. American-Maize Products Co.*, 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988).

In applying the above legal tenets to this case, it is apparent that the Examiner has not established the requisite motivational element. The Examiner specifically asserted that “one of ordinary skill in the art would have found it obvious to modify the processor of Hammond to include a cache bypass around the instruction cache of Hammond so that instructions can be selected from either the output of the translator or the instruction cache based on a cache hit/miss in order to reduce the delay associated with a fetch to memory on an instruction cache miss” (see paragraphs 6 and 10 of the Office Action) (emphasis added).

In response, Applicant stresses that Hammond’s processor does not have any delay issue associated with a cache miss. Hammond et al. discloses as follows: “Instruction cache 542 stores the instructions until they are decoded and executed. At the appropriate time for decoding instructions, instructions in instruction cache 542 are transmitted to decoder 543 for decoding of instructions from instruction cache 542.” Column 15, lines 21-26. Instruction cache 542 is used like a buffer.

In more detail, the Examiner asserted motivation is to include a cache bypass around the instruction cache of Hammond to reduce the delay associated with a cache miss. However, since there is no cache miss in Hammond et al., it is not necessary to have such a cache bypass. Applicant, therefore, emphasizes that avoiding any delay associated with a cache miss does not impel one having ordinary skill in the art to modify Hammond’s processor.

Applicant further explains why there is no motivation to modify Hammond's processor. Hammond et al. discloses a processor system intended to execute an instruction set even if the instruction set is any of a first instruction set and a second instruction set. The first instruction set is an instruction set different from the second instruction set. In Fig. 5 showing a processor, both of the first instruction set and the second instruction set are stored in an external memory. In the first instruction set mode, a translator operates to translate the first instruction set into the second instruction set, and in the second instruction set mode, the instructions of the second instruction set are transferred directly to the processor from the external memory without passing through the translator so that the instructions are executed by an execution unit.

The instructions of the second instruction set are decoded so as to be executed by the execution unit in both the first instruction set mode and the second instruction set mode. A demultiplexer is used to switch an instruction transfer path in accordance with a signal produced by the decoder decoding a switch instruction (jmpx instruction) between the first instruction set mode and the second instruction mode.

In Fig. 5 of Hammond, the instructions of the second instruction set are normally stored in an instruction cache. Hammond et al. does not switch the instructions between the first instruction set and the second instruction set with reference to addresses in accordance with the address from the execution unit.

The Examiner asserted that application of the bypass mechanism as taught by IBM to Hammond's processor system would reduce a delay penalty in cache miss. However, the instruction cache of Hammond is equivalent to an instruction buffer, and there is no possibility of occurrence of the cache miss. Delay may be introduced when a branch instruction is executed in a program sequence and the branch is taken to perform jumping to the branch target instruction.

Even in such branch being taken, it is believed that cache miss/hit is not determined in the instruction cache of Hammond et al. because the instruction cache fetches the instructions at the target from the instruction memory (external memory). Therefore, there is no need to make selection between the output of the external memory and the output of the instruction cache, and thus, no one would be motivated to combine IBM and Hammond.

As described above, Hammond fails to show the determination of whether an instruction to be accessed by the processor is stored in the instruction cache by retrieving the instruction from the instruction cache in accordance with the address from the execution unit. In addition, Hammond does not require caching of instructions in the instruction cache to determine the cache miss or hit in accordance with the address from the execution unit, because the instructions to be used between the first instruction set and the second instruction set are set by the instruction set mode select signal generated by the decoder decoding the switch instruction or “jmpx” instruction.

For **independent claim 16**, it is submitted that the applied combination of Hammond et al. and IBM does not teach a data processing apparatus including all the limitations recited in claim 16.

In paragraph 11 of the Office Action, the Examiner asserted that the claimed first and second instruction storage units are disclosed in Hammond et al. However, the Examiner overlooked the following limitations: “store an instruction in a second instruction architecture transferred from said processor through said bus” for the first instruction storage unit, and “store an instruction in said first instruction architecture transferred from said processor through said bus” for the second instruction storage unit (emphasis added).

Hammond et al. discloses one memory for storing instructions of the first instruction set and instructions of the second instruction set. However, Hammond et al. does not teach transferring instructions from a processor to the memory through a bus. Therefore, the applied combination does not teach each and every limitations recited in independent claim 16.

Based upon the foregoing, Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention in independent claims 1, 12 and 16 for lack of the requisite factual basis and want of the requisite realistic motivation. For dependent claims 2-11, 14, 18 and 19, we may argue that those claims are patentably distinguishable at least because they include all the limitations recited in independent claims 1, 12 and 16, respectively. Applicant, therefore, submits that the imposed rejection of claims 1, 5, 12, 16, 18 and 19 under 35 U.S.C. §103 for obviousness predicated upon Hammond et al. in view of IBM is not factually or legally viable and, hence, respectfully solicits withdrawal thereof.

**Claims 2, 3 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hammond et al. in view of IBM, and further in view of Dickol et al.; claim 4 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Hammond et al. in view of IBM and Dickol et al. and further in view of Goettelmann et al.; claims 6 and 7 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hammond et al. in view of IBM, and further in view of Goettelmann et al.; claims 8 and 10 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hammond et al. in view of IBM, and further in view of Gregor; claims 9 and 11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hammond et al. in view of IBM and Gregor, and further in view of**

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**Schacham et al.; and claim 14 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Hammond et al. in view of IBM, and further in view of Mallick.**

In response, the above-mentioned claims are patentably distinguishable at least because they include all the limitations recited in independent claims 1 and 12, respectively, which are not obvious over the applied combination of Hammond et al. and IBM. Applicant further submits that additional references, Dickol et al., Goettelmann et al., Gregor, Schacham et al. and Mallick do not cure the deficiencies of Hammond et al., as discussed above.

Accordingly, Applicant respectfully solicits withdrawal of the rejection of the claims, and favorable consideration thereof.

**Conclusion.**

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Recognition under 37 C.F.R. 10.9(b)

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